HardCopy IV GX ASIC Product Table

v0.123	HardCopy IV GX ASIC		Stratix IV GX FPGA Prototype		HardCopy IV GX Resource (Stratix IV GX FPGA Prototype Max Resource)[1]								
HardCopy Base Die	Package[2] (Body Size)	Generic Part Number	Prototyping Device	LEs	ASIC Gates[3]	I/O Pins[4]	Full Duplex LVDS Pairs[5]	Transceivers 6.5+Gbps[6]	18x18 Multipliers	PLLs	Total Embedded Memory Bits[7]	M9Ks	M144Ks
HC4GX15	LAF780 (29 mm)	HC4GX15LAF780N	EP4SGX70DF29 (F780)	72.6K	2.8 M	372	28	8+0	384	3	6.3 M	462	16
			EP4SGX110DF29 (F780)	105.6K	3.8 M	372	28	8+0	512	3	8.1 M	660	16
			EP4SGX180DF29 (F780)	175.75K	6.7 M	372	28	8+0	920	3	8.6 M (11.2 M)	660 (950)	20
			EP4SGX230DF29 (F780)	228K	9.2 M	372	28	8+0	1,288	3	8.9 M (13.9 M)	660 (1,235)	22
	LF780 (29 mm)	HC4GX15LF780N	EP4SGX290FH29 (H780)	291.2K	7.7 M	257 (289)	0	8+0 (16+0)	832	2 (4)	9.2 M (13.3 M)	660 (936)	24 (36)
			EP4SGX360FH29 (H780)	353.6K	9.4 M	257 (289)	0	8+0 (16+0)	1,040	2 (4)	9.2 M (16.0 M)	660 (1,248)	24 (36)
HC4GX25	LF780 (29 mm)	HC4GX25LF780N	EP4SGX290FH29 (H780)	291.2K	7.7 M	289	0	16+0	832	4	13.3 M	936	36
			EP4SGX360FH29 (H780)	353.6K	9.4 M	289	0	16+0	1,040	4	13.3 M (17.7 M)	936 (1,248)	36 (48)
	LF1152 (35 mm)	HC4GX25LF1152N	EP4SGX110FF35 (F1152)	105.6K	3.8 M	372	28	16+0	512	4	8.1 M	660	16
			EP4SGX180FF35 (F1152)	175.75K	6.7 M	564	44	16+0	920	6	11.0 M (11.2 M)	936 (950)	20
			EP4SGX230FF35 (F1152)	228K	9.2 M	564	44	16+0	1,288	6	11.3 M (13.9 M)	936 (1,235)	22
			EP4SGX290FF35 (F1152)	291.2K	7.7 M	564	44	16+0	832	6	13.3 M	936	36
			EP4SGX360FF35 (F1152)	353.6K	9.4 M	564	44	16+0	1,040	6	13.3 M (17.7 M)	936 (1248)	36 (48)
	FF1152 (35 mm)	HC4GX25FF1152N	EP4SGX180HF35 (F1152)	175.75K	6.7 M	564	44	16+8	920	6	11.0 M (11.2 M)	936 (950)	20
			EP4SGX230HF35 (F1152)	228K	9.2 M	564	44	16+8	1,288	6	11.3 M (13.9 M)	936 (1,235)	22
			EP4SGX290HF35 (F1152)	291.2K	7.7 M	564	44	16+8	832	6	13.3 M	936	36
			EP4SGX360HF35 (F1152)	353.6K	9.4 M	564	44	16+8	1,040	6	13.3 M (17.7 M)	936 (1,248)	36 (48)
			EP4SGX530HH35 (H1152)	531.2K	11.5 M	564	44	16+8	1,024	6	13.3 M (20.3 M)	936 (1,280)	36 (64)
HC4GX35	FF1152 (35 mm)	HC4GX35FF1152N	EP4SGX230HF35 (F1152)	228K	9.2 M	564	44	16+8	1,288	6	13.9 M	1,235	22
			EP4SGX360HF35 (F1152)	353.6K	9.4 M	564	44	16+8	1,040	6	17.7 M	1,248	48
			EP4SGX530HH35 (H1152)	531.2K	11.5 M	564	44	16+8	1,024	6	20.3 M	1,280	64
	FF1517 (40 mm)	HC4GX35FF1517N	EP4SGX180KF40 (F1517)	175.75K	6.7 M	744	88	24+12	920	8	11.2 M	950	20
			EP4SGX230KF40 (F1517)	228K	9.2 M	744	88	24+12	1,288	8	13.9 M	1,235	22
			EP4SGX290KF40 (F1517)	291.2K	7.7 M	744	88	24+12	832	8	13.3 M	936	36
			EP4SGX360KF40 (F1517)	353.6K	9.4 M	744	88	24+12	1,040	8	17.7 M	1,248	48
			EP4SGX530KH40 (H1517)	531.2K	11.5 M	744	88	24+12	1,024	8	20.3 M	1,280	64

1. Number outside of () indicates available resource in HardCopy device, number inside () indicates maximum resource in FPGA
2. LF and LAF: cost-optimized flip-chip package type; FF: performance-optimized flip-chip package type
3. Calculated as 12 gates per LE plus 5,000 gates per 18 x 18 multiplier. Do not include RAMs, PLLs, test circuitry, and I/O registers.
4. I/O pin count does not include high-speed transceiver serial interface, but does include dedicated clock inputs which can also be used as data inputs: HC4GX15LAF780 has 4 (CLK1N, CLK1P, CLK3N, CLK3P); HC4GX15LF780 and HC4GX25LF780 have 1 (CLK1P); device in F1152 package has 4 (CLK1N, CLK1P, CLK10N, CLK10P); device in F1517 package has 8 (CLK1N, CLK1P, CLK3N, CLK3P, CLK8N, CLK8P, CLK10N, CLK10P)."
5. Each LVDS pair has one TX channel and one RX channel with DPA and soft CDR support
6. Transceivers (PMA and PCS) + CMU transceivers (PMA only); performance may increase upon characterization
7. Memory bit count does not include MLAB memories which are constructed with HCells; 1 Mb = 1,024 x 1,024 bits

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